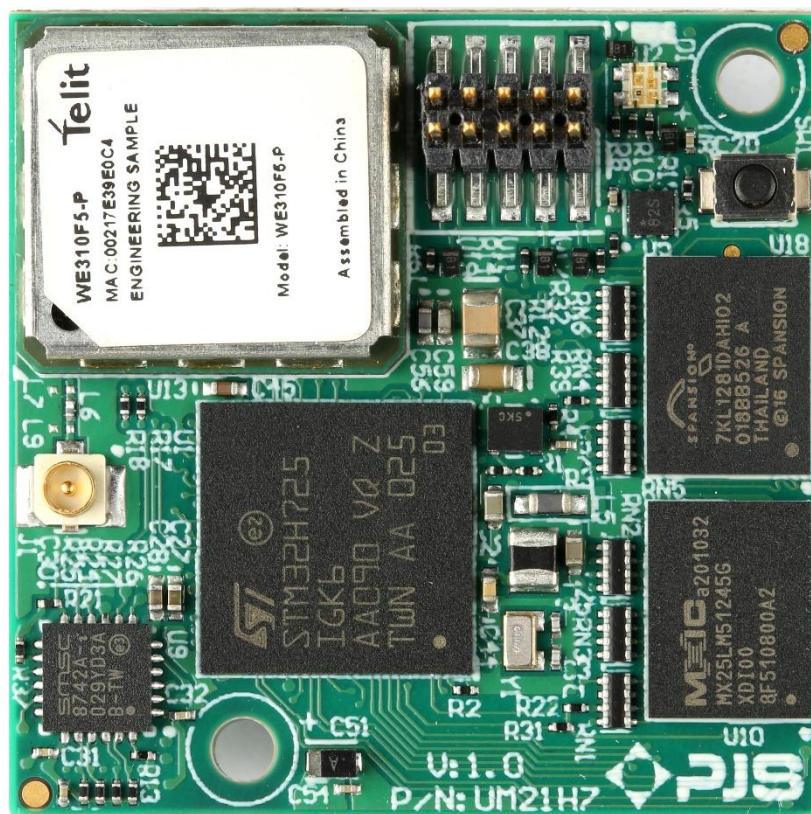




UM21H7 v1.0 Datasheet

ST - STM32H725IG - based System-on-Module

Project Service S.r.l.

UM21H7-STM32 Datasheet

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UM21H7 v1.0 Datasheet

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1. Introduction

This document describes the hardware architecture of the UM21H7-STM32 SOM.

The UM21H7-STM32 is a high-performance System-on-Module and is intended to provide a flexible platform for embedded application that require an ideal building block that easily integrates powerful graphics, rich connectivity and as well as high-processing power.

The UM21H7-STM32 is based on the ST Microelectronic STM32H725 versatile, low-power, high-integration microcontroller.

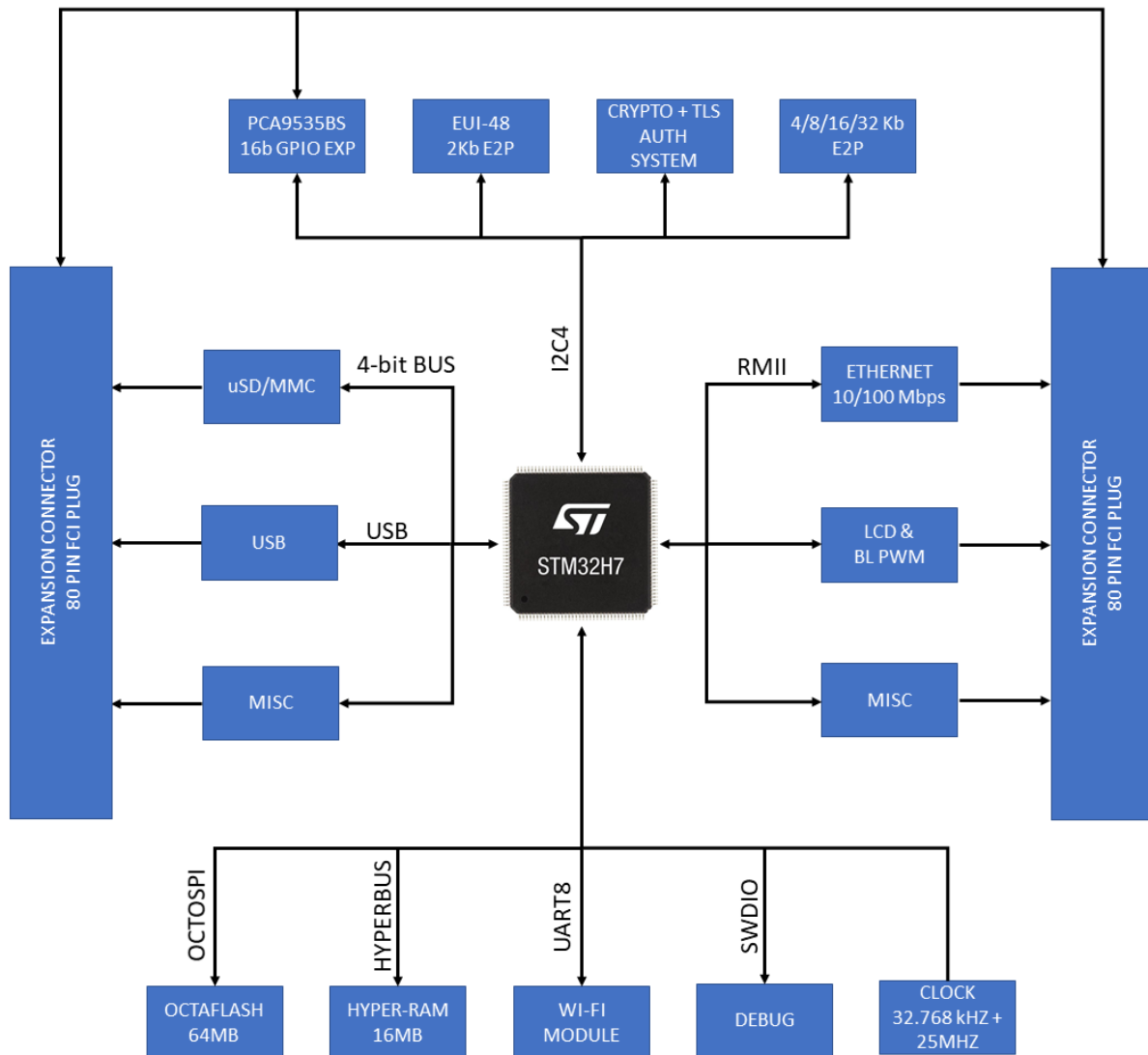
2. Reference Documents

ID	Doc. Name	Date	Revision
RD1			
RD2			
RD3			
RD4			
RD5			
RD6			
RD7			
RD8			

3. Features Summary

- ST Microelectronic STM32H725 (32-bit ARM® Cortex™-M7 Core, up to 550 MHz)
- 16 MB HyperRAM
- 64 MB OctaSPI NOR Flash for storage memory
- Real-Time Clock (RTC)
- 24bit LCD-TFT interface up to XGA resolution
- On-board 10/100 Mbps Ethernet PHY
- On-board Single Band Wi-Fi/BLE5 Module
- 1 x USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip FS PHY
- 1 x uSD card host interface
- Serial interfaces (SPI, I2C, UART)
- 2 x FDCAN Bus Interfaces
- On-board 2K bits I2C™ Serial EEPROM with EU-48™ Node Identity
- On-Board 32K bits I2C™ Serial EEPROM
- On-board I2C™ Cryptographic co-processor with secure hardware-based key storage
- On-board I2C™ 16-bit, low power, I/O expander
- External Interface using two 80-pin 0.4mm pitch connectors
- Single 3.3V power supply
- 30mm x 30mm compact module
- Mounting holes reducing the risk of connector-to-PCB intermittence
- Compliant with the Restriction of Hazardous Substances (RoHS) directive

4. Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the UM21H7 SOM.

5.1 ST Microelectronic STM32H725

The STM32H725 device is based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 550 MHz frequency.

The Cortex®-M7 core features a floating-point unit (FPU) which supports all ARM® double-precision and single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

It also features standard and advanced communication interfaces.

- Five I2Cs
- Six SPIs, four I2Ss in half-duplex mode.
- Five USARTs plus five UARTs and one LPUART
- A USB OTG high-speed with full-speed capability (with the ULPI),
- Two FDCANs plus one TT-FDCAN interface
- Two SAI serial audio interfaces
- Two SDMMC interfaces
- Ethernet interface
- MDIO slaves
- 24-bit parallel digital RGB LCD-TFT display controller up to XGA resolution
- Chrom-ART Accelerator™.
- SPDIF-Rx interface with four inputs
- One SWPMI (Single Wire Protocol Master Interface)
- HDMI-CEC

5.2 Memory

5.2.1 HyperRAM

The UM21H7 SOM is equipped with 16MB Cypress HyperRAM memory running @100MHz with Double-Data Rate (DDR).

The S70KL1281DABHI023 device is a high-speed CMOS, self-refresh Dynamic RAM (DRAM), with a HyperBus interface in a dual-die stack of 64-Mb HyperRAM devices in a single package.

HyperBus is a low-signal-count, Double Data Rate (DDR) interface that achieves high-speed read and write throughput.

The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals.

A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM core with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals.

5.2.2 Non-volatile Storage Memory

5.2.2.1 OctoSPI NOR Flash

The UM21H7 SOM provides 64 MB OctoSPI NOR Flash memory, using the Macronix MX25LM51245G device. MX25LM51245G is 512Mb bits Octal interface Serial NOR Flash memory, which is configured as 67,108,864 x 8 internally.

MX25LM51245G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

A different version of UM21H7 SOM mounts 64 MB OctoSPI NOR Flash memory, using the Cypress S28HL512TFPBHI010.

The Cypress Semper™ Flash Octal family of products are high-speed CMOS, 45-nm MirrorBit NOR flash devices that are compliant with the JEDEC JESD251 eXpanded SPI (xSPI) specification.

Semper Flash with Octal Interface devices support both the Octal Peripheral Interface (OPI) as well as Legacy x1 Serial Peripheral Interface (SPI).

Both interfaces serially transfer transactions reducing the number of interface connection signals.

5.2.2.2 EUI-48™ Node Identity

The UM21H7 SOM equips the Microchip 24AA025E48 a 2 Kbit Electrically Erasable PROM. The device is organized as two blocks of 128 x 8-bit memory with a 2-wire serial interface.

The 24AA025E48 is programmed at the factory with a globally unique, EUI-48™ and EUI-64™ compatible node address stored in the upper half of the array and permanently write-protected.

The remaining 1,024 bits are available for application use.

5.2.2.3 Serial EEPROM

The UM21H7 SOM equips the Microchip 24AA04 a 4K Electrically Erasable PROM.

The device is organized as two blocks of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.7V, with standby and active currents of only 1 µA and 1 mA, respectively.

The 24AA04 also has a page write capability for up to 16 bytes of data.

5.3 I/O port Expander

The UM21H7 SOM is equipped with a 16-bit I / O expander in order to manage control signals internal to the SOM and drive the standard periphery without the need to use the microcontroller's pin.

The PCA9535 is a 24-pin CMOS device that provide 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I2C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I2C-bus I/O expanders.

The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging.

Usable I/O expander pins are available on CN2 expansion connector.

5.4 10/100 Ethernet PHY

The UM21H7 SOM features the LAN8742A-CZ a low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3 and 802.3u standards.

The LAN8742A/LAN8742Ai supports communication with an Ethernet MAC via a standard RMII interface.

It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) operation.

The LAN8742A/LAN8742Ai implements auto- negotiation to automatically determine the best possible speed and duplex mode of operation. HP Auto-MDIX support allows the use of direct connect or cross-over LAN cables. Integrated Wake on LAN (WoL) support provides a mechanism to trigger an interrupt upon reception of a perfect DA, broadcast, magic packet, or wakeup frame.

The LAN8742A/LAN8742Ai supports both IEEE 802.3-2005 compliant and vendor-specific register functions. However, no register access is required for operation. The initial configuration may be selected via the configuration pins. Register-selectable configuration options may be used to further define the functionality of the transceiver.

The LAN8742A/LAN8742Ai can be programmed to support wake-on-LAN at the physical layer, allowing detection of configurable Wake-up Frame and Magic packets.

This feature allows filtering of packets at the PHY layer, without requiring MAC intervention.

Additionally, the LAN8742A/LAN8742Ai supports cable diagnostics which allow the device to identify opens/shorts and their location on the cable via vendor-specific registers.

5.5 WiFi/BLE5 Module

The UM21H7 SOM includes the Telit WE310F5-P Wi-Fi/BLE5 module, a fully integrated, single-band Wi-Fi (802.11 b/g/n 2.4GHz) and Bluetooth Low Energy (BLE5) combination module that provides a low-cost and highspeed wireless connection to an embedded microcontroller over UART, SPI and SDIO interfaces.

Based on Realtek Ameba system on chip (SoC), the WE310F5 is ideal for a wide variety of embedded devices, including smart lighting, home appliances, medical wearables, smart city sensors, aftermarket telematics and industrial robots.

A UMCC RF connector is included in order to improve Wi-Fi/BLE5 module performance connecting an external antenna.

5.5.1 Update/Debug connector

WE310F5-P Wi-Fi/BLE5 module can be updated or debugged using an external connector, CN4, placed on UM21H7 SOM.

CN4 is a 5pin, 1.00mm pitch connector, 665105131822 from Würth Elektronik.

Recommended mating connector is the 665005113322 from Würth Elektronik.

CN4 Pin-Out:

Signal	Pin #	Type	Description
DBG_TXD	1	O	Auxiliary (DEBUG) UART output
DBG_RXD	2	I	Auxiliary (DEBUG) UART input
EN	3	I	ENABLE pin
DOWNLOAD	4	I	Flash Mode enabling when Low
GND	5	POWER	Ground

6. External Connectors

The UM21H7 SOM exposes two 80 pin 0.4mm pitch connectors.

The recommended mating connector for baseboard interfacing are:

- DF40HC(4.0)-80DS-0.4V(51)

In addition to the two 80 pin interface UM21H7 SOM exposes a 10-pin, 1.27mm pitch, pin header for SWDIO interface

Pin#:

Pin number on the FCI connector

Pin Name:

Default UM21H7 SOM pin name

Type:

Pin type & direction:

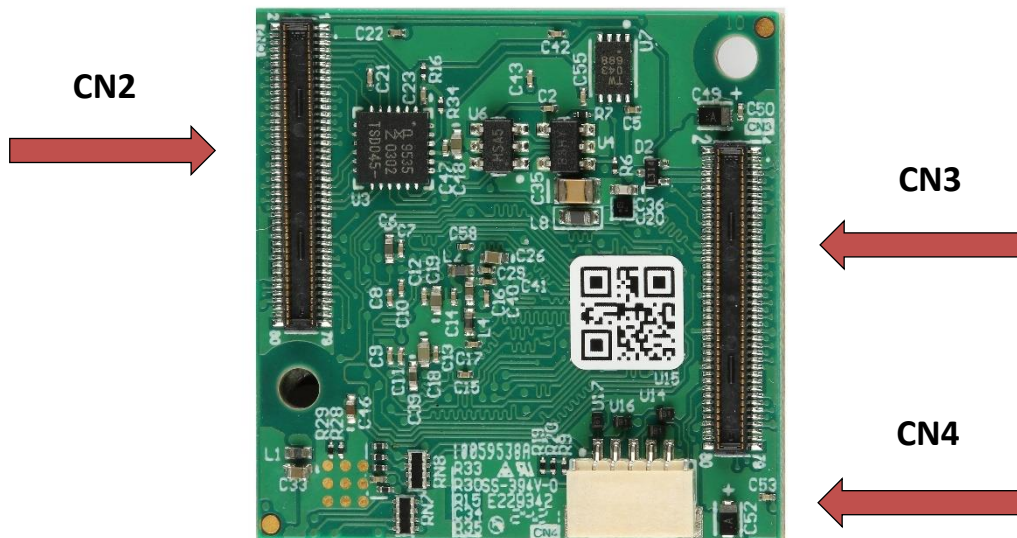
- I – In
- O – Out
- DS – Differential Signal
- A – Analog
- Power – Power Pin

Pin Group:

Pin functionality group

STM32H725 Ball:

Ball number



6.1 UM21H7 SOM Connectors Pin-out

6.1.1 CN2 Connector:

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
1	GND	POWER	Digital GND		
2	GND	POWER	Digital GND		
3	EXP_GPIO1	I/O	From GPIO EXPANDER		
4	EXP_SWDIO	I/O	System debug SWDIO pin	PA[13]	B13
5	EXP_GPIO2	I/O	From GPIO EXPANDER		
6	EXP_SWCLK	I/O	System debug SWCLK pin	PA[14]	A12
7	EXP_GPIO3	I/O	From GPIO EXPANDER		
8	EXP_RST	I	System debug Reset pin	NRST	L1
9	EXP_GPIO4	I/O	From GPIO EXPANDER		
10	PA0_C	I/O // A	General purpose / ADC	PA[0_C]	R3
11	EXP_GPIO5	IO	From GPIO EXPANDER		
12	PA1_C	I/O // A	General purpose / ADC	PA[1_C]	P3
13	EXP_GPIO6	I/O	From GPIO EXPANDER		
14	PA2_C	I/O // A	General purpose / ADC	PC[2_C]	N1
15	EXP_GPIO7	I/O	From GPIO EXPANDER		
16	PA3_C	I/O // A	General purpose / ADC	PC[3_C]	N2
17	BOOT0	I	BOOT selection pin		C5
18	PG15	I/O	General purpose	PG[15]	D7
19	PC13	I/O	General purpose	PC[13]	C1
20	PG4	I/O	General purpose	PG[04]	G14
21	PB6	I/O	General purpose	PB[06]	A5
22	PH2	I/O	General purpose	PH[02]	N4
23	PB7	I/O	General purpose	PB[07]	B5
24	PE8	I/O	General purpose	PE[08]	N8
25	PF5	I/O	General purpose	PF[05]	H3
26	PB3	I/O	General purpose	PB[03]	A6
27	PD3	I/O	General purpose	PD[03]	A9
28	PE10	I/O	General purpose	PE[10]	R9
29	PB15	I/O	General purpose	PB[15]	K14
30	PE9	I/O	General purpose	PE[09]	R11
31	PC2	I/O	General purpose	PC[02]	M1
32	PA5	I/O	General purpose	PA[05]	P6
33	GND	POWER	Digital GND		
34	PD14	I/O	General purpose	PG[14]	C7
35	PB8	I/O	General purpose	PB[08]	A2
36	PB4	I/O	General purpose	PB[04]	B6

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
37	PD1	I/O	General purpose	PD[01]	A10
38	GND	POWER	Digital GND		
39	GND	POWER	Digital GND		
40	uSD_CLK	O	uSD CLK pin	PC[12]	B11
41	uSD_CD	I/O	uSD Card Detect – from GPIO EXP		
42	uSD_CMD	I/O	uSD CMD pin	PD[02]	B10
43	uSD_PWR_EN	O	uSD Power enable – from GPIO EXP		
44	uSD_D3	I/O	uSD D3 pin	PC[11]	C11
45	uSD_OC_FLT#	O	uSD OC FAULT – from GPIO EXP		
46	uSD_D2	I/O	uSD D2 pin	PC[10]	C12
47	USB_OC_FLT#	O	USB OC FAULT – from GPIO EXP		
48	uSD_D1	I/O	uSD D1 pin	PC[09]	E13
49	uSD_PWR_EN	O	USB Power enable – from GPIO EXP		
50	uSD_D0	I/O	uSD D0 pin	PC[08]	D14
51	GND	POWER	Digital GND		
52	GND	POWER	Digital GND		
53	PD8	I/O	General purpose	PD[08]	L14
54	OTG_FS_ID	I	USB 5V indication	PA[10]	C14
55	PD9	I/O	General purpose	PD[09]	K13
56	OTG_FS_VBUS	I	USB 5V indication	PA[09]	D13
57	PB14	I/O	General purpose	PB[14]	K15
58	GND	POWER	Digital GND		
59	PD11	I/O	General purpose	PD[11]	J13
60	OTG_FS_P	DS	USB HS in FS mode positive signal	PA[12]	B15
61	GND	POWER	Digital GND		
62	OTG_FS_N	DS	USB HS in FS mode negative signal	PA[11]	C15
63	PD12	I/O	General purpose	PD[12]	J15
64	GND	POWER	Digital GND		
65	PD13	I/O	General purpose	PD[13]	H15
66	ETH_TX_P	DS	Ethernet PHY positive transmit signal		
67	PE3	I/O	General purpose	PE[03]	B2
68	ETH_TX_N	DS	Ethernet PHY negative transmit signal		
69	GND	POWER	Digital GND		
70	GND	POWER	Digital GND		
71	ETH_LED1/LINK	O	Ethernet LED/Link		
72	ETH_RX_P	DS	Ethernet PHY positive receive signal		
73	ETH_LED2/SPEED	O	Ethernet LED/Speed		
74	ETH_RX_N	DS	Ethernet PHY negative receive signal		
75	GND	POWER	Digital GND		
76	GND	POWER	Digital GND		

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
77	3V3	POWER	3.3 V power supply IN		
78	3V3	POWER	3.3 V power supply IN		
79	3V3	POWER	3.3 V power supply IN		
80	3V3	POWER	3.3 V power supply IN		

6.1.2 CN3 Connector:

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
1	3V3	POWER	3.3 V power supply IN		
2	3V3	POWER	3.3 V power supply IN		
3	3V3	POWER	3.3 V power supply IN		
4	3V3	POWER	3.3 V power supply IN		
5	GND	POWER	Digital GND		
6	GND	POWER	Digital GND		
7	nRST	I	System RESET pin	NRST	L1
8	VBAT_IN	POWER	RTC backup battery IN		E2
9	PF7	I/O	General purpose	PF[07]	J3
10	PC3	I/O	General purpose	PC[03]	M2
11	PF11	I/O	General purpose	PF[11]	N7
12	PE15	I/O	General purpose	PE[15]	P14
13	PH7	I/O	General purpose	PH[07]	M11
14	PB10	I/O	General purpose	PB[10]	N12
15	PE7	I/O	General purpose	PE[07]	P9
16	PH5	I/O	General purpose	PH[05]	R5
17	GND	POWER	Digital GND		
18	GND	POWER	Digital GND		
19	LCD_BL_EN	O	LCD-BACKLIGHT ENABLE from GPIO EXP		
20	LCD_BL	O	LCD-BACKLIGHT CONTROL	PE[14]	M12
21	GND	POWER	Digital GND		
22	GND	POWER	Digital GND		
23	LCD_HSYNC	I/O	LCD-TFT Interface HSYNC	PC[06]	E14
24	LCD_CLK	O	LCD-TFT Interface CLK	PG[07]	G13
25	GND	POWER	Digital GND		
26	GND	POWER	Digital GND		
27	LCD_VSYNC	I/O	LCD-TFT Interface VSYNC	PA[04]	P5
28	LCD_DE	I/O	LCD-TFT Interface DE	PE[13]	P13
29	GND	POWER	Digital GND		
30	GND	POWER	Digital GND		
31	LCD_B0	O	LCD-TFT Interface B0	PE[04]	B1
32	LCD_B4	O	LCD-TFT Interface B4	PE[12]	P12

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
33	LCD_B1	O	LCD-TFT Interface B1	PD[00]	C10
34	LCD_B5	O	LCD-TFT Interface B5	PB[05]	C6
35	LCD_B2	O	LCD-TFT Interface B2	PD[06]	D9
36	LCD_B6	O	LCD-TFT Interface B6	PA[15]	A11
37	LCD_B3	O	LCD-TFT Interface B3	PA[08]	B14
38	LCD_B7	O	LCD-TFT Interface B7	PB[09]	B3
39	GND	POWER	Digital GND		
40	GND	POWER	Digital GND		
41	LCD_G0	O	LCD-TFT Interface G0	PE[05]	D3
42	LCD_G4	O	LCD-TFT Interface G4	PH[15]	D12
43	LCD_G1	O	LCD-TFT Interface G1	PE[06]	E3
44	LCD_G5	O	LCD-TFT Interface G5	PH[04]	P4
45	LCD_G2	O	LCD-TFT Interface G2	PH[13]	C13
46	LCD_G6	O	LCD-TFT Interface G6	PC[07]	D15
47	LCD_G3	O	LCD-TFT Interface G3	PH[14]	B12
48	LCD_G7	O	LCD-TFT Interface G7	PG[08]	G12
49	GND	POWER	Digital GND		
50	GND	POWER	Digital GND		
51	LCD_R0	O	LCD-TFT Interface R0	PG[13]	B7
52	LCD_R4	O	LCD-TFT Interface R4	PH[10]	N14
53	LCD_R1	O	LCD-TFT Interface R1	PH[03]	R4
54	LCD_R5	O	LCD-TFT Interface R5	PC[00]	L2
55	LCD_R2	O	LCD-TFT Interface R2	PH[08]	N13
56	LCD_R6	O	LCD-TFT Interface R6	PB[01]	M8
57	LCD_R3	O	LCD-TFT Interface R3	PH[09]	M14
58	LCD_R7	O	LCD-TFT Interface R7	PG[06]	F14
59	GND	POWER	Digital GND		
60	GND	POWER	Digital GND		
61	PD10	I/O	General purpose	PD[10]	L13
62	PD15	I/O	General purpose	PD[15]	J12
63	VSSA	A	Analog GND	VSSA	N3
64	PD14	I/O	General purpose	PD[14]	H14
65	VREF	A	Analog VREF	VREF+	M3
66	PH6	I/O	General purpose	PH[06]	P15
67	GND	POWER	Digital GND		
68	PA0	I/O	General purpose	PA[00]	P1
69	PB0	I/O	General purpose	PB[00]	R8
70	PH11	I/O	General purpose	PH[11]	M13
71	PA3	I/O	General purpose	PA[03]	N5
72	PH12	I/O	General purpose	PH[12]	N15

Pin #	Pin Name	Type	Pin Group	GPIO	STM32H725 Ball
73	PA6	I/O	General purpose	PA[06]	R7
74	PF13	I/O	General purpose	PF[13]	N11
75	GND	POWER	Digital GND		
76	GND	POWER	Digital GND		
77	3V3	POWER	3.3 V power supply IN		
78	3V3	POWER	3.3 V power supply IN		
79	3V3	POWER	3.3 V power supply IN		
80	3V3	POWER	3.3 V power supply IN		

6.2 80 pin Connector Pin Mux

The table below summarizes the additional available functionality for each pin- of two 80 pin FCI connector.

6.2.1 CN2 Connector Pin Mux:

PIN	GPIO	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
10	PA[0_C]	ADC	TIM2_CH1	TIM5_CH1				
12	PA[1_C]	ADC						
14	PC[2_C]	ADC						
16	PC[3_C]	ADC						
18	PG[15]	GPIO						
19	PC[13]	RTC_COMP						
20	PG[04]	GPIO						
21	PB[06]	I2C1_SCL	USART1_TX	TIM4_CH1	CAN2_TX			
22	PH[02]	GPIO						
23	PB[07]	I2C1_SDA	USART1_RX	TIM4_CH2				
24	PE[08]	UART7_TX	TIM1_CH1N					
25	PF[05]	GPIO						
26	PB[03]	UART7_RX	I2S1_CK	SPI2_SCK	TIM2_CH2			
27	PD[03]	SPI2_SCK	SPI2_CLK		I2S2_CK			
28	PE[10]	UART7_CTS	TIM1_CH2N					
29	PB[15]	SPI2_MOSI	SPI2_MOSI	USART1_RX	I2S2_SDO			
30	PE[09]	UART7_RTS	TIM1_CH1					
31	PC[02]	SPI2_MISO						
32	PA[05]	SPI6_SCK	TIM2_CH1	DAC1_OUT2	TIM8_CH1N			
34	PG[14]	SPI6_MOSI	USART6_TX		I2S6_SDO			
35	PB[08]	CAN1_TX	I2C1_SCL					
36	PB[04]	SPI6_MISO	I2S1_SDI	SPI2_MISO	I2S6_SDI			
37	PD[01]	CAN1_RX	UART4_TX					
40	PC[12]	uSD_CLK	I2S3_SDO	UART5_TX	SPI3_MOSI			
42	PD[02]	uSD_CMD						

PIN	GPIO	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
44	PC[11]	uSD_D3	I2S3_SDI		SPI3_MISO			
46	PC[10]	uSD_D2	I2S3_CK		SPI3_SCK			
48	PC[09]	uSD_D1	TIM3_CH4	UART5_CTS	TIM8_CH4			
50	PC[08]	uSD_D0	TIM3_CH3	UART5_RTS	TIM8_CH3			
53	PD[08]	USART3_TX						
55	PD[09]	USART3_RX						
57	PB[14]	USART3_RTS	SPI2_MISO	USART1_TX	I2S2_SDI			
59	PD[11]	USART3_CTS						
63	PD[12]	ENC_TIM4_CH1	CAN3_RX	UART5_RX				
65	PD[13]	ENC_TIM4_CH2	CAN3_TX					
67	PE[03]	GPIO						

6.2.2 CN3 Connector Pin Mux:

PIN	GPIO	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
9	PF[07]	SPI5_SCK	UART7_TX	TIM17_CH1	TIM23_CH2			
10	PC[03]	ADC						
11	PF[11]	SPI5_MOSI	TIM24_CH1					
12	PE[15]	GPIO						
13	PH[07]	SPI5_MISO						
14	PB[10]	I2C2_SCL						
15	PE[07]	GPIO	UART7_TX					
16	PH[05]	I2C2_SDA						
20	PE[14]	LCD_BL	TIM1_CH4					
23	PC[06]	LCD_HSYNC	TIM3_CH1	TIM_8_CH1				
24	PG[07]	LCD_CLK						
27	PA[04]	LCD_VSYNC	I2S3_WS	DAC1_OUT1				
28	PE[13]	LCD_DE	TIM1_CH3					
31	PE[04]	LCD_B0	TIM15_CH1N					
32	PE[12]	LCD_B4	SPI4_SCK	TIM1_CH3N				
33	PD[00]	LCD_B1	CAN1_RX					
34	PB[05]	LCD_B5	I2S1_SDO	SPI2_MOSI	CAN2_RX			
35	PD[06]	LCD_B2						
36	PA[15]	LCD_B6	I2S1_WS	TIM2_CH1	I2S6_WS			
37	PA[08]	LCD_B3	I2C3_SCL	TIM1_CH1				
38	PB[09]	LCD_B7	I2C1_SDA	TIM4_CH4	I2S2_WS			
41	PE[05]	LCD_G0	SPI4_MISO	TIM15_CH1				
42	PH[15]	LCD_G4	TIM8_CH3N					
43	PE[06]	LCD_G1	SPI4_MOSI	TIM15_CH2				
44	PH[04]	LCD_G5	ADC					

PIN	GPIO	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6
45	PH[13]	LCD_G2	CAN1_TX	TIM8_CH1N				
46	PC[07]	LCD_G6	USART6_RX	TIM8_CH2	TIM3_CH2			
47	PH[14]	LCD_G3	UART4_RX	TIM8_CH2N				
48	PG[08]	LCD_G7	USART6_RTS					
51	PG[13]	LCD_R0	USART6_CTS	TIM23_CH2	I2S6_CK			
52	PH[10]	LCD_R4	TIM5_CH1					
53	PH[03]	LCD_R1	ADC					
54	PC[00]	LCD_R5						
55	PH[08]	LCD_R2	I2C3_SDA					
56	PB[01]	LCD_R6	TIM1_CH3N	TIM3_CH2	TIM8_CH3N			
57	PH[09]	LCD_R3	TIM12_CH2					
58	PG[06]	LCD_R7						
61	PD[10]	GPIO						
62	PD[15]	UART9_TX	TIM4_CH4					
64	PD[14]	UART9_RX	TIM4_CH3					
66	PH[06]	TIM12_CH1						
68	PA[00]	ENC_TIM5_CH1	TIM2_CH1					
69	PB[00]	TIM3_CH3	ADC					
70	PH[11]	ENC_TIM5_CH2						
71	PA[03]	TIM2_CH4	ADC					
72	PH[12]	TIM5_CH3						
73	PA[06]	TIM3_CH1	ADC	TIM13_CH1				
74	PF[13]	TIM24_CH3	ADC					

6.3 Unavailable Signals of STM32H7

The following signals are not available on the output connectors:

- I2C4, used to connect the GPIO Expander, EEPROMs and CRYPTO;
- OctoSPI, used to connect the Flash Memory;
- HyperBus, used to connect the RAM;
- UART8, used to connect the WiFi module.

7. SOM's interfaces

7.1 Display Interface

The UM21H7 SOM provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words.

7.2 Megabit Ethernet

Megabit Ethernet Features:

The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbps Ethernet IEEE 802.3 and IEEE 802.3u networks.

An external Megabit magnetics is required to complete the interface to the media.

Megabit Ethernet Signals (CN2):

Signal	Pin #	Type	Description
ETH_TX_P	66	DS	Positive transmit signal
ETH_TX_N	68	DS	Negative transmit signal
ETH_RX_P	72	DS	Positive receive signal
ETH_RX_N	74	DS	Negative receive signal
ETH_LED1/LINK	71	O	Ethernet LED/Link
ETH_LED2/SPEED	73	O	Ethernet LED/Speed

7.3 USB 2.0 F.S.

The UM21H7 SOM embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support

- External HS or HS OTG operation supporting ULPI in SDR mode The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

USB 2.0 F.S. Signals (CN2):

Signal	Pin #	Type	Description
OTG_FS_P	60	DS	Positive USB F.S data
OTG_FS_N	62	DS	Negative USB F.S data
OTG_FS_VBUS	56	I	USB 2.0 VBUS indicator (5V)
OTG_FS_ID	54	I	USB OTG
USB_OC_FLT#	47	O	USB Over Current Fault
USB_PWR_EN	49	O	USB Power Enable

7.4 uSD

The STM32 supports MultiMediaCard System Specification Version 4.51 in three different data bus modes: 1 bit (default), 4 bits and 8 bits.

In this SOM the 4 bits configuration is used.

SDIO Signals (CN2):

Signal	Pin #	Type	Description
SDIO_CLK	40	O	Clock for MMC/SD/SDIO card
SDIO_CMD	42	I/O	CMD line connect to card
SDIO_DATA0	50	I/O	DAT0 line in all modes (also used to detect busy state)
SDIO_DATA1	48	I/O	DAT1 line
SDIO_DATA2	46	I/O	DAT2 line
SDIO_DATA3	44	I/O	DAT3 line

7.5 SPI

The UM21H7 SOM feature up to three SPIs in slave and master modes in full-duplex and simplex communication modes.

SPI2, SPI5, SPI6 allow communicating up to 150 Mbits/s in Master and Slave modes, in Half-duplex, Full-duplex and Simplex modes.

The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits.

The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.

All SPIs can be served by the DMA controller.

7.6 I2C

I2C-1, 2 Interface connectivity peripherals provide serial interface for external devices. Data rates of up to 1 Mbps are supported.

I2C1 Signals (CN2):

Signal	Pin #	Type	Description
I2C1_SCL	21	I/O	I2C1 I2C clock, open drain
I2C1_SDA	23	I/O	I2C1 I2C data, open drain

I2C2 Signals (CN3):

Signal	Pin #	Type	Description
I2C2_SCL	14	I/O	I2C2 I2C clock, open drain
I2C2_SDA	16	I/O	I2C2 I2C data, open drain

7.7 SWDIO

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

In UM21H7 SOM only Serial Wire Debug port is available.

Debug is performed using 3 pins (SWDIO).

SWDIO signals on CN2 Connector:

Signal	Pin #	Type	Description
SWDIO	4	I/O	Bidirectional Data pin
SWCLK	6	I	Clock Signal
RST	8	I	Reset

Note: SWDIO signals are also available on onboard CN1 connector.

7.8 Boot Modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The boot loader is located in non-user System memory.

It is used to reprogram the Flash memory through a serial interface.

7.9 General Purpose IO

Most of the SOM's IO pins can be used as GPIOs.

8. Absolute Maximum Characteristics

Power Supply	Min	Max	Unit
Main Power Supply, DC-IN	-0.3	3.5	V

9. Operational Characteristics

9.1 Power supplies

Power Supply	Min	Typical	Max	Unit
Main Power Supply, DC-IN	-5%	3.3	+5%	V

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